13. The field effect transistor of claim 1 wherein the field effect transistor is a first field effect transistor, further comprising a second field effect transistor coupled in parallel to the first field effect transistor, the second field effect transistor having a second effective width.

14. The field effect transistor of claim 13 wherein the second effective width of the second field effect transistor is smaller than the effective width of the first field effect transistor.

15. The field effect transistor of claim 13 wherein the second effective width of the second field effect transistor is the same as the effective width of the field effect transistor.

REMARKS

Claims 1-15 will be pending upon entry of the present amendment. Claims 1-3 and 6-11 are being amended. Claims 13-15 are being newly presented.

Claims 1-5 and 9-12 were rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 6,232,642 to Yamazaki.

Yamazaki does not teach or suggest the invention recited in claims 1-5 and 9-12, as amended. For example, amended claim 1 recites a filed effect transistor that includes a doped region formed in the substrate and completely surrounding an active region that includes a channel region having an effective width defined by a variable doping profile in a first direction with respect to the doped region. Yamazaki does not disclose a doped region that completely surrounds the active region of a field effect transistor. Instead, Yamazaki employs doped pinning regions 105, 106 that extend only on opposite sides of a channel region 102 and do not completely surround an active region comprised of a source region 101, the channel region 102, and a drain region 103. Accordingly, claim 1 is not anticipated by Yamazaki.

Claims 2-5 and new claims 13-15 depend on claim 1, and thus, are also not anticipated by Yamazaki.

Yamazaki also does not disclose the invention recited in claims 9-12, as amended. Amended claim 9 recites a field effect transistor that includes a first doped region extending along an entire first side of the active area; and a second doped region extending along an entire second side of the active area. Yamazaki does not disclose such first and second doped regions that extend along entire first and second sides, respectively of an active area. As discussed above, the pinning regions 105, 106 are positioned only on opposite sides of the channel area 102 and do not extend along the entire sides of the active area that includes the source and drain regions 101, 103. As a result, the pinning regions 105, 106 do not provide the same measure of isolation from other transistors that is provided by the first and second doped regions of the claimed invention. Accordingly, claims 9-12 are not anticipated by Yamazaki.

Claims 6-8 were rejected under 35 U.S.C. § 103 as being unpatentable over Yamazaki in view of EP patent application 442,413 of Iwazaki.

Yamazaki and Iwazaki do not teach or suggest the invention recited in claims 6-8. Claims 6-8 recite first and second field effect transistors that are coupled in parallel with each other. Yamazaki does not teach two field effect transistors in the same circuit. Iwazaki shows two transistors Q1, Q2, but they are not coupled *in parallel* with each other. Rather, the transistors Q1, Q2 are coupled in series with each other. Nothing in the prior art provides a motivation for modifying the transistors Q1, Q2 to place them in parallel with each other. Further, Yamazaki and Iwazaki do not suggest how one would place them in parallel. According, claims 6-8 are nonobvious in view of the cited prior art.

The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

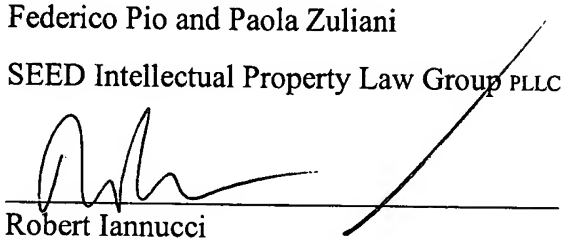
Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version With Markings to Show Changes Made.**"

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

Federico Pio and Paola Zuliani

SEED Intellectual Property Law Group PLLC



Robert Iannucci
Registration No. 33,514

RXI:kkh

Enclosure:
Postcard

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 1-3 and 6-11 are being amended as follows:

1. (Amended) A field effect transistor integrated on a semiconductor substrate having an active area, the field effect transistor comprising:

a source region and a drain region formed in the semiconductor substrate;

a channel region interposed between said source and drain regions having a predefined nominal width in a first direction that is perpendicular to a second direction that extends through the source, drain, and channel regions, the channel, source, and drain regions together comprising an active region of the substrate; and

a doped region formed in the substrate and completely surrounding the active region, the channel region having an effective width defined by a variable doping profile in the first direction with respect to the doped region.

2. (Amended) The field effect transistor according to claim 1, wherein an interior edge of the ~~variable doping profile is one of a~~doped region ~~implanted adjacent to the transistor~~is spaced laterally from the channel region.

3. (Amended) The field effect transistor according to claim 2, wherein the effective width is a function of a distance of ~~a~~the doped region ~~implanted in~~from the active area.

6. (Amended) ~~The field effect transistor of claim 1 further comprising~~ A transistor structure, comprising:

a first field effect transistor integrated on a semiconductor substrate having an active area, the first field effect transistor including:

a source region and a drain region formed in the semiconductor substrate; and

a channel region interposed between said source and drain regions having a predefined nominal width in a first direction that is perpendicular to a second direction that extends through the source, drain, and channel regions, the channel region having a first effective width defined by a variable doping profile in the first direction; and

a second field effect transistor coupled in parallel to the first field effect transistor, the second field effect transistor having a second effective width.

7. (Amended) The field effect transistor of claim 6 wherein the second effective width of the second field effect transistor is smaller than the first effective width of the first field effect transistor.

8. (Amended) The field effect transistor of claim 6 wherein the second effective width of the second field effect transistor is the same as the first effective width of the first field effect transistor.

9. (Amended) A field effect transistor comprising:

an active area formed in a semiconductor substrate;

a source region and a drain region formed in the active area; ~~and~~

a channel region interposed between said source and drain regions and having a first nominal width in a first direction that is perpendicular to a second direction that extends through the source, drain, and channel regions; the channel region having a variable doping profile in the semiconductor substrate extending in the first direction from no additional dopant in a center of the channel region to a concentrated amount of dopant at edges of the channel region, wherein an effective channel width of the channel region is relative to an amount and concentration of dopant in the channel region;

a first doped region formed in the substrate extending along an entire first side of the active area from a position beyond the source region in the second direction to a position beyond the drain region in the second direction; and

a second doped region formed in the substrate extending along an entire second side of the active area from a position beyond the source region in the second direction to a

position beyond the drain region in the second direction, the second side being opposite to the first side.

10. (Amended) The field effect transistor of claim 9, wherein the first and second doped regions extend beyond third and fourth sides of the active area, the third and fourth sides being opposite to each other and transverse to the first and second sides ~~variable doping profile is one of a region implanted adjacent to the transistor~~.

11. (Amended) The field effect transistor of claim 10, wherein the effective channel width is a function of a distance ~~of a region implanted by the active area~~ between the first and second doped regions.

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